REMARKS

The Examiner has rejected claims 1-5, 7-9, and 14-15 as anticipated under 35 U.S.C. 102 by Okayama U.S. Patent number 6128684.

The Examiner has rejected claims 6, 13, and 16-18 under 35 U.S.C. 103 over Okayama in view of Applicants admitted prior art (AAPA).

The Examiner has rejected claim 10 under 35 U.S.C. 103 over Okayama in view of Acharya, U.S. Patent 6459698; and 11-12 under 35 U.S.C. 103 over Okayama in view of Printz, et. al. U.S. Published Patent Application 2003/0009334.

The edited claims:

Claim 1 has been rewritten to incorporate the limitations of dependent claim 2, and claims depending on claim 1 have been amended to reference claim 1. Similarly, the elements of claims 7 and 8 have been combined into a single edited claim 8. The element of claim 2 has also been incorporated into claim 9. The elements of claims 15 and 16 have been combined into an amended claim 15.

These amendments have been made to clarify that the coherency maintenance apparatus of the present application maintains coherency of the *address translation apparatus* to a memory image; and does not maintain coherency of a cache. While a cache may be present in the bridge, and that cache may have associated coherency maintenance logic, this is not the claimed coherency maintenance apparatus.

35 U.S.C. 102 Rejections

Applicant agrees that Okayama U.S. Patent 6128684 provides many elements of the claimed invention. As the Examiner asserts, Okayama provides an I/O bus bridge with:

1. a first interface to first interconnect apparatus;
2. a second interface to second interconnect apparatus, the second interconnect apparatus of a type capable of connection to peripherals having direct memory access apparatus for transferring data;
3. the bridge capable of serving as a bridge for data transfer between the first interface and the second interface; and

4. address translation hardware coupled to translate I/O virtual addresses received from the second interface into physical memory addresses for transmission onto the first interface.

Okayama fails, however, to provide "the address translation hardware further comprising coherency maintenance apparatus", and more particularly Okayama fails to provide address translation hardware "wherein the coherency maintenance apparatus maintains coherency by observing the first interface for references to entries of a page table in a memory," as claimed in Claim 1 (formerly claim 1 & claim 2).

The examiner has cited Okayama's PTE Renewal Refill Controller (Okayama 6) (PTERRC) as providing this element. While Okayama's PTE Renewal Refill Controller has many functions, it lacks this critical feature.

Okayama has lengthy and detailed description of function of his PTERRC. Okayama's PTERRC has the ability to directly transfer (Okayama col 7 lines 45-65, col 8 lines 35-68, col 9 lines 1-30) elements of a Translation Lookaside Buffer (TLB) image in memory from that memory into the TLB of the bridge. Clearly his PTERRC can flush, and refill from a memory image, the address translation logic from a memory image *when instructed by the processor to do so.*

The problem in the art, of which Okayama is an excellent example, that the present application addresses is that of *automatically maintaining coherency between the TLB of the bridge and an image in system memory when the processor changes the TLB image in memory,* and of doing so without direct processor intervention. It is changes to the TLB image in memory that potentially can lead to the lack of coherency that the "coherency maintenance apparatus" of the present application addresses.

Okayama does not disclose or suggest any ability of the PTERRC to observe the memory bus for writes to TLB locations, and thus not only fails to provide coherency maintenance apparatus for the TLB, but fails to provide coherency by observing the first interface for references to entries of an I/O page table (or TLB image) in memory as claimed.

Without this element of coherency maintenance apparatus to keep the TLB of the bridge in synchronization with the TLB image in memory, Okayama fails to anticipate the claimed invention under 35 U.S.C. 102 (b).

35 U.S.C. 103 Rejections

The Examiner has rejected claims 6, 13, and 16-18 under 35 U.S.C. 103 over Okayama in view of Applicants admitted prior art (AAPA).

As stated in the paragraph 13 of the disclosure, as AAPA, snoop logic has become common for maintaining coherency of cache memory. When a first processor writes to system memory, cache systems of a second processor may see that write and invalidate or replace corresponding entries (if any) present in that cache. Similarly, in paragraph 14 Applicant discussed directory based systems for coherency maintenance of cache.

In the rejections, the Examiner makes repeated reference to maintenance of coherency of a cache as if that were what is claimed. Applicant notes that the present claims make no reference to coherency of a *cache*, what is claimed is maintenance of coherency of *address translation logic* (such as a translation lookaside buffer) to a memory image of desired address translation logic data.

Paragraph 16, however, states that "While snoop-based and directory-based coherency maintenance mechanisms have historically been used to maintain cache coherency, they are not typically used to maintain coherency of address mapping hardware such as TLB's". The AAPA therefore fails to suggest a use of cache-like snoop logic or directory-based coherency maintenance apparatus to maintain coherency of *address translation logic*. Paragraph 12 also states "It is known that the coherency of I/O TLBs with their associated page tables in memory can be maintained through software, and this is common practice in the art," thereby teaching away from the present invention.

While Applicant's application describes the combination of coherency maintenance mechanisms with address translation logic in an I/O to system bus bridge, this is found in Applicant's description of his invention and not as admitted prior art. Absent sufficient elements in prior art, and suggestion in the art *outside Applicant's description of his invention* that these elements be combined, a 35 U.S.C. 103 rejection is improper.

CONCLUSION

Applicant submits that the present 35 U.S.C. 102 and 103 rejections are improper as applied to the amended claims, and respectfully requests that the application as amended be reconsidered.

Applicant's attorney believes that no additional fees are due, but the Commissioner is authorized to charge any additionally required fees to deposit account 08-2025. Applicant's attorney urges Examiner to telephone if a conversation could expedite prosecution.

Respectfully submitted,

By: _____

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